

MC100EP16VB

3.3V / 5V ECL Differential Receiver/Driver with High and Low Gain

Description

The EP16VB is a world-class differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices but with both high and low gain outputs. Q_{HG} and \overline{Q}_{HG} outputs have a DC gain several times larger than the DC gain of an EP16. \overline{Q} output is provided for feedback purposes.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Special considerations are required for differential inputs under No Signal conditions to prevent instability.

The 100 Series contains temperature compensation.

Features

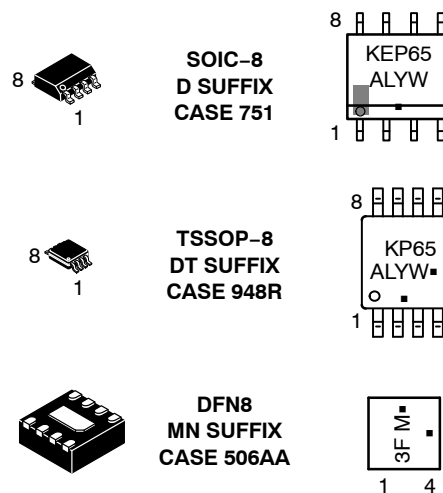
- Gain > 200
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: $V_{CC} = 3.0$ V to 5.5 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -5.5 V
- V_{BB} Output
- Pb-Free Packages are Available



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<http://onsemi.com>

MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

MC100EP16VB

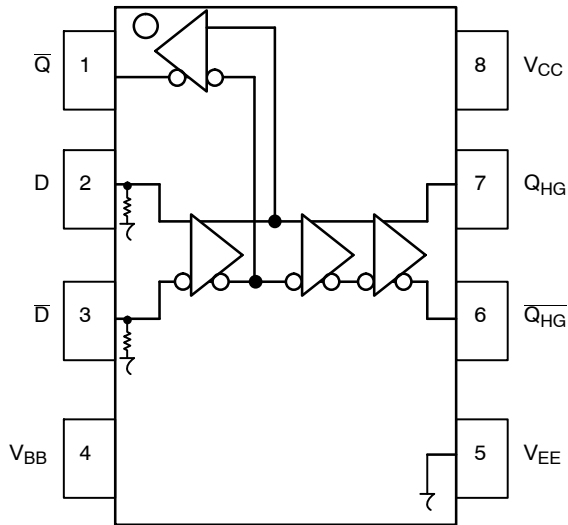


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
D*, $\overline{D^*}$	ECL Data Inputs
\overline{Q}	ECL Data Output
Q_{HG} , $\overline{Q_{HG}}$	ECL High Gain Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

*Pins will default LOW when left open.

Table 2. ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor	75 k Ω	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model	> 4 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	SOIC-8	Level 1
	TSSOP-8	Level 1
	DFN8	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	167 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MC100EP16VB

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 SOIC	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	8 TSSOP	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T _{sol}	Wave Solder Pb Pb-Free			265 265	°C
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	27	37	47	22	30	38	24	32	40	mA
V _{OH}	Output HIGH Voltage (Note 4)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V _{OL}	Output LOW Voltage (Note 4)	1305	1430	1555	1305	1400	1555	1305	1380	1555	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V _{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V _{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	2045	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -2.2 V.

4. All loading with 50 Ω to V_{CC} - 2.0 V.

5. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC100EP16VB

Table 5. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	22	30	38	24	32	40	mA
V_{OH}	Output HIGH Voltage (Note 7)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 7)	3005	3130	3255	3005	3100	3255	3005	3080	3255	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{BB}	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0 V to -0.5 V.

7. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

8. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 9)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	22	30	38	24	32	40	mA
V_{OH}	Output HIGH Voltage (Note 10)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 10)	-1995	-1870	-1745	-1995	-1900	-1745	-1995	-1920	-1745	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 11)	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Input and output parameters vary 1:1 with V_{CC} .

10. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

11. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC100EP16VB

Table 7. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V to } -5.5\text{ V}$ or $V_{CC} = 3.0\text{ V to } 5.5\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 12)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 2)		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay (Differential) \overline{Q} (Differential) QHG, $\overline{QH\overline{G}}$ (Single-Ended) \overline{Q} (Single-Ended) QHG, $\overline{QH\overline{G}}$	200 200 250 250	275 280 325 330	350 350 400 400	250 250 300 300	300 300 350 350	400 400 450 450	275 275 325 325	310 320 360 370	425 425 475 475	ps
t_{SKEW}	Duty Cycle Skew (Note 13)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	Cycle-to-Cycle Jitter (Figure 3)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential) HG (Differential) \overline{Q}	25 150	800 800	1200 1200	25 150	800 800	1200 1200	25 150	800 800	1200 1200	mV
t_r , t_f	Output Rise/Fall Times (20% - 80%) \overline{Q} QHG, $\overline{QH\overline{G}}$	200 70	270 130	400 220	220 80	300 150	420 240	250 100	310 170	450 270	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

13. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

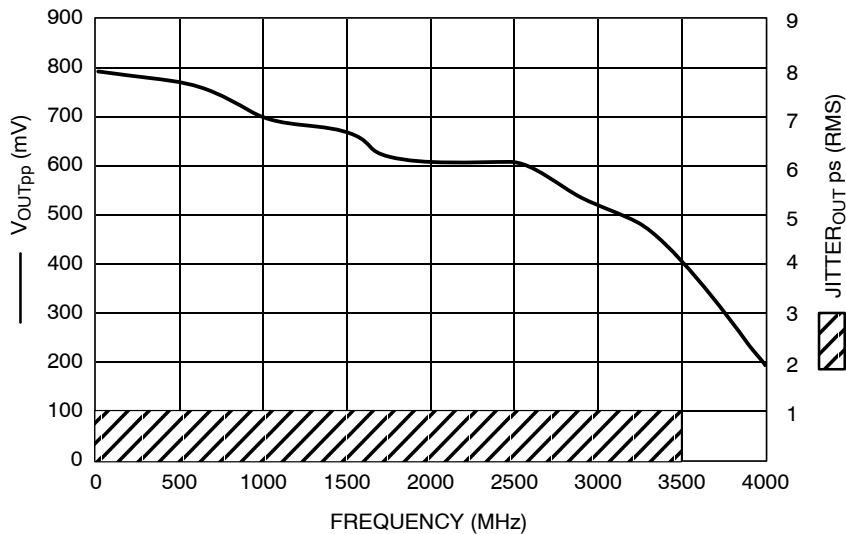


Figure 2. F_{max} /Jitter for QHG, $\overline{QH\overline{G}}$ Output

MC100EP16VB

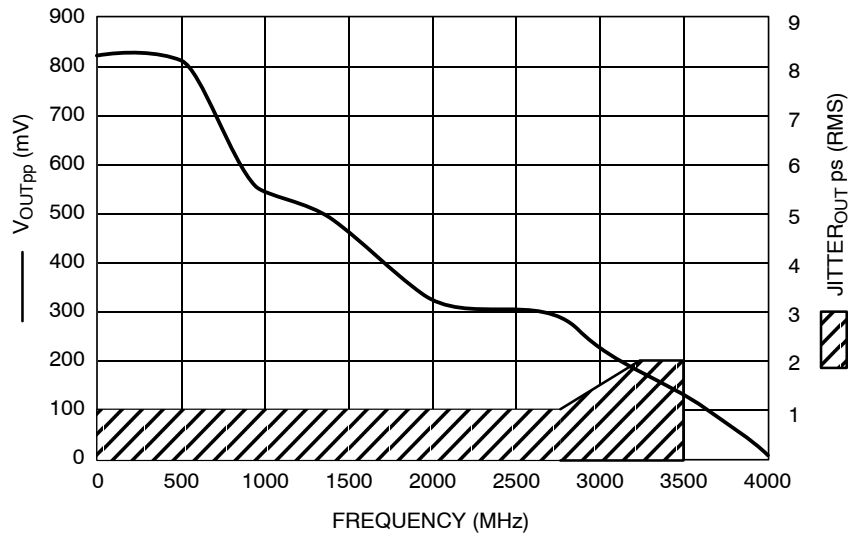


Figure 3. F_{max}/Jitter for Q̄ Output

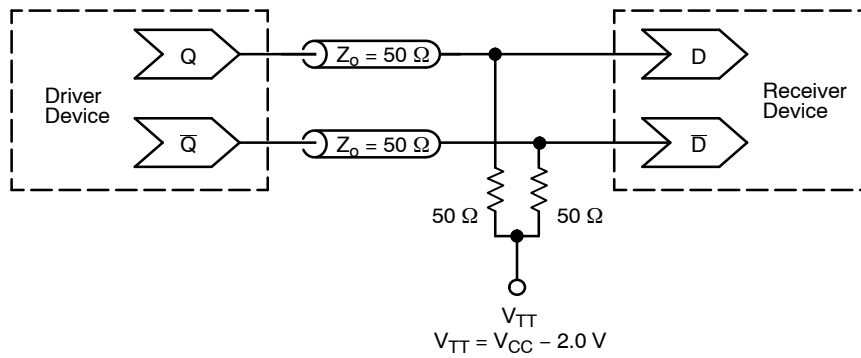


Figure 4. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

MC100EP16VB

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP16VBD	SOIC-8	98 Units / Rail
MC100EP16VBDG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100EP16VBDR2	SOIC-8	2500 / Tape & Reel
MC100EP16VBDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100EP16VBDT	TSSOP-8	100 Units / Rail
MC100EP16VBDTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EP16VBDR2	TSSOP-8	2500 / Tape & Reel
MC100EP16VBDR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EP16VBMNR4	DFN8	1000 / Tape & Reel
MC100EP16VBMNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

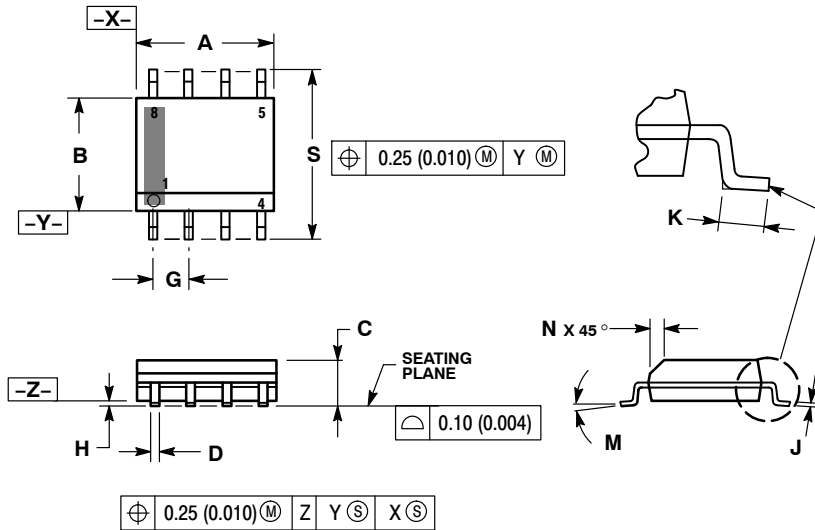
Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

MC100EP16VB

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AJ

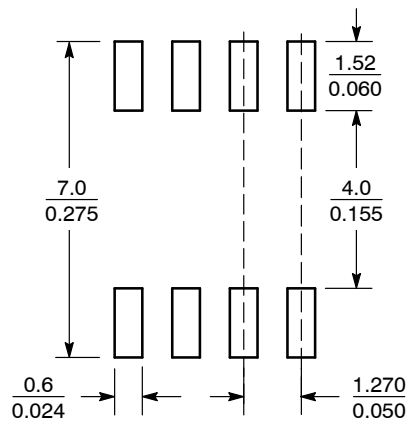


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



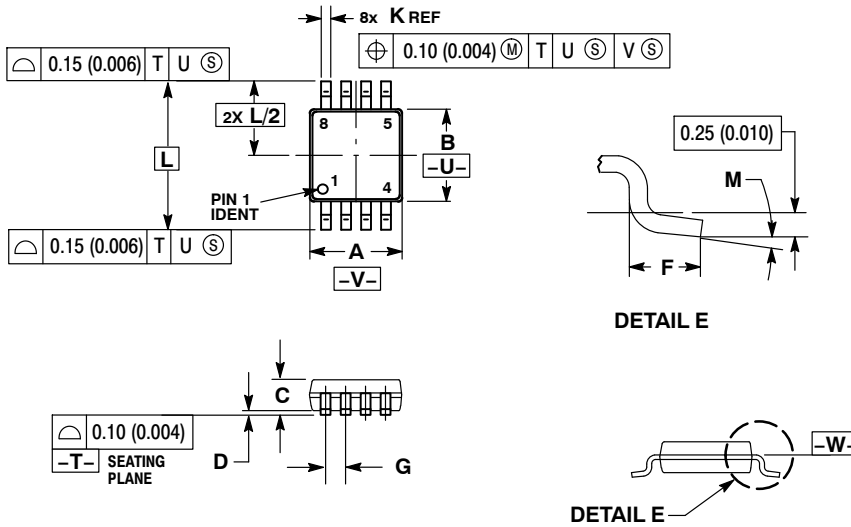
SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC100EP16VB

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



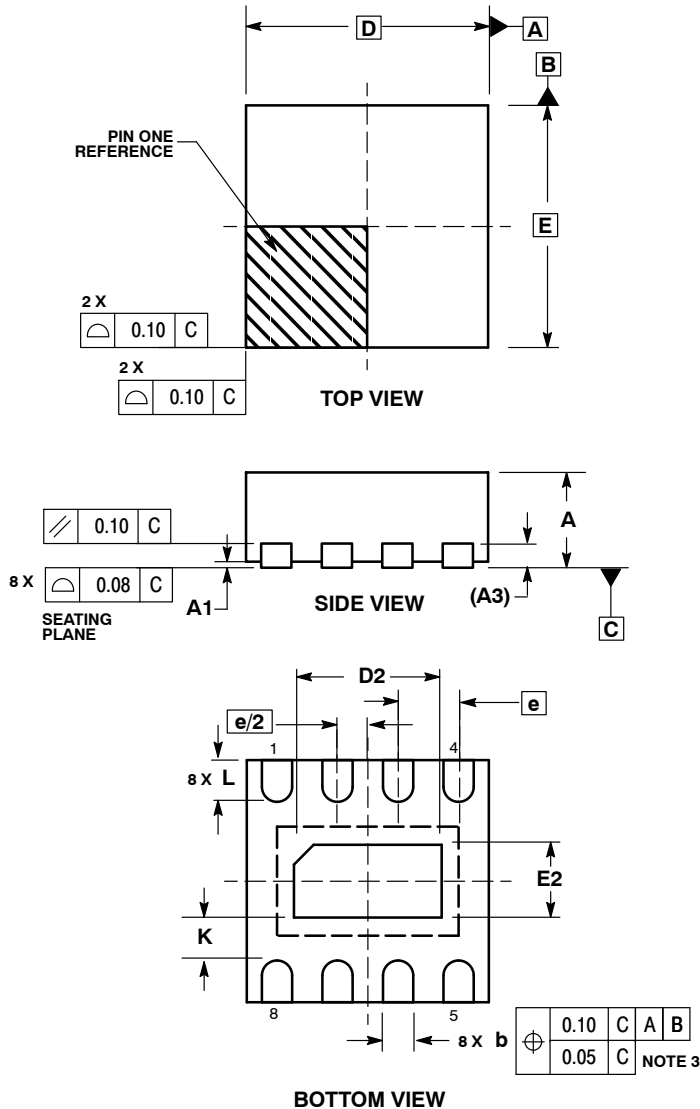
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

MC100EP16VB

PACKAGE DIMENSIONS

DFN8
CASE 506AA-01
ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

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